UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,866	01/16/2004	Craig Hansen	43876-156	5955

7590 02/21/2007

McDERMONTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
COLEMAN, ERIC	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,866	HANSEN ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 28-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 28-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8,10-17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen (patent No. 5,751,614).

3. Cohen taught the invention as claimed including a data processing ("DP") system comprising:

a) Decoding a single instruction writing data to destination register specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data (ME, MB) contained in the register (e.g., see col. 7, lines 34-59);

b) Detecting some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields (e.g., see col. 5, lines 21-col. 6 line 34 and figs. 3,4); and

c) Writing the write-enabled data fields to a specified destination register location (e.g., see col. 5, lines 46-57).

4. Cohen did not expressly detail that the data that was stored in the destination register was stored in memory. Cohen taught RISC system. In RISC system it was well known in the art when there were more variables than could be held in the registers the excess data was held in memory. Consequently in at least one implementation of the Cohen teachings one of ordinary skill would have been motivated to store the data produced by the single instruction in memory at least when the there were not enough registers to store the data.

5. As to the addition limitations of claims 10, Cohen taught the instructions performed comprised RISC instructions and the multiplex instruction is the instruction discussed above (e.g., see fig. 3)

6. As to claims 2,11, Cohen taught each of the fields of the mask having a width of one bit (e.g., see fig. 3) [each bit field with a "1" comprised one bit].

7. As to claims 3,12, Cohen taught each of fields of the data contained in the register has a register has a width of one bit (e.g., see fig. 3)[each bit of the mask corresponded to a one bit field of the register].

8. As to claims 4,13, Cohen taught the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled fields to the specified memory location (e.g., see fig. 3) [the unaltered fields outside of the mask field that corresponded to the zeros of the mask].

9. As to claims 5,14, Cohen taught the mask is contained in a specified register (the mask in one form is contained in the instruction register containing the instruction in

fig.3) specified by the instruction address and also the mask is in a temporary register (e.g., see col. 5, lines 47-57).

10. As per claim 6,15, Cohen did not specify that the memory location was contained in a specified register. However since in the occurrence that the registers were full and excess data was stored in memory one of ordinary skill would have been motivated to store a pointer to the memory location in the registers (such as a stack) at least to provide quick access to the address to access the data stored in memory. Also since in the RISC system the system operates on data stored in registers to provide speed of processing so one of ordinary skill encountering the not enough register would have been motivated to store a pointer in the register to the memory location of the data stored in memory for quick access to the data.

11. As per claim 7,16, Cohen did not teach the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address. However conventional memory comprises a specified memory width (although there are various widths of different memories) one of ordinary skill would have been motivated to store the width of the memory at least to allow the system properly set up the access to the data for properly performing the rotate and merge operations. This allows for compatibility with upgrading of the memory.

12. As per claim 8, Cohen taught the predetermined logic value is a "1" (e.g., see fig. 3)[the "1s" in the mask].

13. Claims 9,18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claims 1-8 above, and further in view of Kabir (patent No. 5,933,160).

14. As per claim 9, 18 Kabir taught decoding a second single instruction specifying a fourth register containing a plurality of floating point operands; multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products; and providing the partitioned field of a result as a concatenated result (e.g., see fig. 4, 5a, 5b and col. 8,lines 21-45).

15. It would have been obvious to one of ordinary skill to combine the teachings of Cohen and Kabir. Both references were directed toward performing operations of partial widths of data stored in registers. Kabir taught further operations to be performed on the partial width data such as multiplication on floating point data (e.g., see fig. 4) for performing image processing in a digital system (e.g., see col. 1, lines 6-11) consequently one of ordinary skill would have been motivated to incorporate the floating point operations to the Cohen system at least to provide the capability use in addition applications such as graphics applications.

Claims 28-32,35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen.

Cohen taught the invention substantially as claimed including a data processing ("DP") system comprising (as per claims 28,35):

a) decoding a single instruction for performing a bitwise insert operation on data in registers in a register file within a programmable processor, the bitwise operation

operating on a first operand and a second operand stored in the register file (e.g., see col. 7, lines 34-59); and for each bit in the first operand, the bitwise insert operation inserting the bit into a corresponding bit position in a destination value if a corresponding bit in the second operand has a first predetermined value register (e.g., see col. 5, lines 21-col. 6 line 34 and figs. 3,4);

Cohen did not expressly detail (claim 28,35) that the registers were in a register file. However the organizing of registers into a file where each could be address in a predetermined manner using an register location or address was well known in the art at the time of the claimed invention. One of ordinary skill would have been motivated to implement the registers as part of a register file at least to facilitate access to the data where storing data in registers can be accessed more quickly than when data is stored in slower memory.

As per claim 29,36 Cohen taught the predetermined logic value is a "1" (e.g., see fig. 3)[the "1s" in the mask].

16. As per claims 30,31,32, 37,38,39 Cohen taught the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled fields to the specified memory location (e.g., see fig. 3) [the unaltered fields outside of the mask field that corresponded to the zeros of the mask].

17. Claims 33,34,40,41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claims 28,35 above, and further in view of Kabir.

18. As per claims 33,40 Kabir taught arithmetic operation where operands were stored in registers of 64-bit width (e.g., see col. 8, lines 5-37 and col. 9, line 27-col. 10, line 28 and fig.5A,5B). As to the operand being 64 bit width one of ordinary skill would have been motivated to use data with more bits such as 64, 128 etc to take advantage of the increasing capacity of industry standard memories, data paths and processors at the time of the claimed invention.

19. It would have been obvious to one of ordinary skill to combine the teachings of Cohen and Kabir. Both references were directed toward performing operations of partial widths of data stored in registers. Kabir taught further operations to be performed on the partial width data such as multiplication on floating point data (e.g., see fig. 4) for performing image processing in a digital system (e.g., see col. 1, lines 6-11) consequently one of ordinary skill would have been motivated to incorporate the floating point operations to the Cohen system at least to provide the capability use in addition applications such as graphics applications.

As per claim 34, Kabir taught executing a plurality of different group floating point operation that arithmetically operate on multiple floating point operands partitioned in fields of an operand register in the plurality of registers to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result comprises a plurality of individual floating point results (e.g., see fig. 4, 5a, 5b and col. 8,lines 21-45 and col. 5, lines 6-47 and col. 4, lines 23-64).

As per claim 41, Kabir taught instructions further comprises a plurality of different group floating-point arithmetic operations that arithmetically operate one multiple

floating-point operands stored in partitioned fields of an operand register in the plurality of registers to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result comprises a plurality of individual floating-point results (e.g., see col. 4, lines 23-61 and col. 7, line 7-col. 8, line 41).

Response to Arguments

Applicant's arguments filed 11/21/06 have been fully considered but they are not persuasive.

The applicant argues that the priority for the instant application includes the '840 patent (and its appendix). The Examiner has reviewed the '840 patent and the (appendix to the '599 patent which is linked the '840 patent by a dependency chain that comprises a continuation in part). The Examiner contends that the operation of the '599 patent performs transferring portions of register via a data path that is narrower than the register used by the instruction execution means. The portions of the operand are stored into the register and an operation is performed on the data. However the masking or bitwise insertion operation is not taught and no means for a single instruction to perform this complex operation is taught by the '599 or '840 patents. Also the use of masking bit means is in neither patent teachings where the '599 and 840 patent merely sequentially store data in a register from a data path. The is no masking means to selectively separately determine whether one bit or bits is to be inserted while other means are used to determine whether the other bits of destination receive bit or bits. Therefore there is no support for the masking or bitwise insert operation. Without

any teachings for bitwise insert or masking means the storing is merely conventional storing such as shifting in data into a memory location. The parent patents do not even provide bit lines so direct storage of data to a portion of the destination this is further evidence there could not be any means to selectively inhibit or allow storing individual bit or bits to the location where the bit or bits are intended to be stored. Consequently the other features claimed are not taught or supported by the '840 or 599 patents. As to the appendices the Examiner as reviewed the portions indicated in the applicant's remarks and cannot find support for the features claimed. Therefore the Examiner concludes that the priority for the claimed invention does not extend to the '599 or the '840 patents.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER